REMARKS

I. STATUS OF CLAIMS

In accordance with 37 C.F.R. § 1.173(c), the status of the claims are as follows:

Claims 1-33 and 40-54 are pending in the reissue application.

Claims 1-33 are original claims and remain allowed. No changes have been made to claims 1-33. **In this regard, the Examiner mistakenly stated in the outstanding Office Action that claims 1-33 were canceled. Claims 1-33 were never canceled.**

Claims 34-54 were previously added in the preliminary amendment filed November 24, 2003, with claims 34-39 being canceled in the amendment filed November 20, 2006.

Claims 40 and 47 are being amended in the enclosed amendment.

No new matter has been added.

II. EXPLANATION OF SUPPORT IN DISCLOSURE FOR AMENDMENTS

Claims 40 and 47 have been amended respectively as follows "wherein the decoding unit is capable of decoding a plurality of instructions executed in parallel" and "a decoding unit that decodes [[the]] a plurality of instructions executed in parallel." Same as for the previous amendment, support for the aforementioned feature of the present invention can be found, for example, in Figures 4, 7 and 11 of Applicants' drawings and the corresponding disclosure in Applicants' specification.

III. PRIOR ART REJECTION

Claims 40-54 stand rejected under 35 U.S.C. § 102 as being anticipated by Sato et al. '710 ("Sato"). Claims 40 and 47 are independent. This rejection is respectfully traversed for the following reasons.

Claims 40 and 47 embody an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than M * N bits; where M is the maximum bit length of an instruction that can be executed in parallel and N is the number of instructions that can be executed in parallel. Claim 40 recites in pertinent part, "wherein the decoding unit is capable of decoding a plurality of instructions executed in parallel" and claim 47 recites in pertinent part, "a decoding unit that decodes a plurality of instructions executed in parallel." In order to read Sato on the claimed invention, the Examiner broadly interprets the bus width of the bus formed between INSTRUCT LATCH 211 and FORMAT DECODER 221 as being 16 bits to be shorter than 16*4 = 64 bits. In so doing, the Examiner has necessarily interpreted the decoder 221 as the ***entire*** decoder in of itself. However, in reality, element 221 is merely one part of a decoder made up of elements 221, 222, 223, 224, 231, 232, 233, 234 ***collectively***. When interpreted this way, Sato does not disclose "the total bit width of the instruction bus is shorter than M * N bits." Accordingly, the claims have been amended as noted above, that is, to embody a decoding unit which is capable of decoding a plurality of instructions executed in parallel. In contrast, the interpreted decoder 221 of Sato can only decode a single instruction, so that Sato does not disclose the combination of features recited in the pending claims.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by

probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Sato docs not anticipate claims 40 and 47, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 40 and 47 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

III. CONCLUSION

Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in

connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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